UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,508	06/24/2003	John E. Smee	020515	2193

7590 10/18/2006

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
CORRIELUS, JEAN B	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,508	SMEE ET AL.	
	Examiner	Art Unit	
	Jean B. Corrielus	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7 and 9-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 4, 13 and 18-21 are objected to because of the following informalities: claim 4, line 4, "the" should be inserted before "chips". The limitation "estimates", recited in claim 7, line 2 is not consistent with claim 5 that recites "estimate".

Claim 13, line 1, "a" should be replaced by "the". The same comment applies to claim 18, line 10 and claim 19, line 2 "a chip" claim 21, line 3 "a more" and "a sliced". Note that any claim whose base claim is objected is likewise objected.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14, lines 7-8 "the chip" lacks of proper antecedent basis. Dependent claims 13-17 are likewise rejected.

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 4, 9-17and 20-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 4 recites in line 2, "estimates **for a subset** of the plurality of chips" however the specification, as filed does not provide support for such limitation as claimed.

The same comment applies to claim 6 with respect to the limitation "**a portion** of the encoded symbol", claim 9 and 14, the limitation of "**an identification of the chip** based in part on a correlation to **one** or more chips in the code" and "noise component based in part on the **one or more chip identification** output from the slicer", claim 10 and claim 11 "chip **identification** values"; claim 20 the limitation "noise component based in part on **one** or more sliced chips"; claim 22, the limitation of "**an identification of the sliced chip** based in part on a correlation among the plurality of chips in the codeword" and "noise component based in part on the **identification** of the sliced chip"; claim 24, the limitations recited, in lines 1-4 and claim 25, the limitations ""**identify a chip value** based in part on a correlation among at least **a portion of chips**" and "**chip value** from the slicer".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 4-7, 9-14,16-22 and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Webster et al US Patent No. 6,233,273.

As per claim 1, Webster et al discloses a method and apparatus comprising receiving a frame see fig. 5 in a digital communications stream, the frame having a training portion see col. 10, lines 20-21 and a data portion see for instance output of decision 105, wherein the data portion comprises inherently an encoded symbol, the encoded symbol having a plurality of code words see fig. 5 wherein each code word has a plurality of chips see col. 7, lines 46-50 and col. 8, lines 3-6, slicing a chip from the encoded symbol using "chip decision" 76; removing interference from the chip using feedback filter 75 ; deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word (i. e. output of matched filter 33 inherently includes correlation among the chips) using the combiner 73; and providing the more accurate symbol estimate (i. e. output of combiner 73) as input to the chip decision 76 (chip slicer) that determines an updated estimate of the encoded symbol based on the more accurate estimate from the sliced chip..

As per claim 2, the receiving step (inherently) has to receive the encoded symbol during the data portion of the frame.

As per claim 4, Webster teaches a more accurate sliced chip estimates are derived for each codeword see fig. 5 and because of the inherent correlation among the chips, at least 50% of the more accurate sliced chip estimates have to be inherently based on the correlation among the chips in the codeword.

As per claim 5, the more accurate symbol estimate are provided to the feedback filter and the estimate are stored in the taps of the feedback filter 75 via decision device 76.

As per claim 6, the removing step includes combining an output of the feedback filter with a portion of the encoded symbol, see fig. 5 for improved performance in removing interference from the sliced chip.

As per claim 7, see claim 4.

As per claim 9, Webster et al teaches a chip decision circuit 76 (chip slicer) for extracting a chip from a code word, the code word received as part of an encoded symbol in a digital communication stream see fig. 5 the chip slicer configured to determine an estimate of an identification of the chip based in part on a correlation to one or more chips in the codeword (note that signal stream includes an inherent correlation among the chips, hence the estimate has to be based on the correlation among the chips); a feed back filter 75 configured to determine a noise component based in part on the one or more chip identification output from the slicer 76, the feedback filter 75 having a plurality of content registers see fig. 8 to store identification values; and a combiner 73 (chip combiner) configured to derive a more accurate symbol estimate based on the noise component from the feedback filter 75, wherein the

combiner 73 (chip combiner) provides improved symbol estimates to the chip decision 76 (chip slicer).

As per claim 10 the taps (content registers) are updated with more accurate symbol chip identification values based (during) decision directed updating (i. e as provided by decision circuit 76) note that the value(s) stored in the taps change(s) as the decision circuit 76 provides new (updated) output signal.

As per claim 11, the content registers of the feedback filter contain chip identification values based on correlation among chips in the codeword e claim 7.

As per claim 12, the feedback filter75 uses FIR filter wherein the FIR subtracts out postcursor intersymbol interference from the current slicer input see col. 8, lines 12-20 and col. 9, lines 51-54.

As per claim 13, see claim 1.

As per claim 14, Webster teaches a preprocessor 33 for carrying out signal processing tasks; and providing a feed forward filter 71 with baseband samples the feed forward filter 71 for processing the baseband samples and for sending a digital data stream to a chip (decision) slicer 76 in combination with any signal added or subtracted by a chip combiner 73, the chip slicer configured to determine an estimate of an identification of the chip based in part on a correlation to one or more chips in the codeword (note that signal stream includes an inherent correlation among the chips, hence the estimate has to be based on the correlation among the chips; and a feedback filter 75 for processing previous chip slicer outputs and derive a noise and provide the

noise component to the chip combiner to subtract out interference from the current input to the chip slicer 76.

As per claim 16, Webster et al teaches the chip slicer 76 is configured to extract a portion of the data stream that corresponds to a single chip see col. 3, line 57 and col. 7, lines 10-12.

As per claim 17, Webster et al further teaches the feedback filter 75 feeds the noise component back into the chip slicer 76 by way of a chip combiner 73 so that the noise component can be subtracted from the next incoming signal from the feed forward filter 71 before the next incoming signal is fed into the chip slicer 76. 18.

As per claim 18, see claim 1.

As per claim 19, Webster et al teaches that the means/step for slicing a chip from the encoded symbol further comprises a chip slicer 76 for extracting a chip from a code word.

As per claim 20 the means for removing interference includes a FB filter 75 having a plurality of taps (content registers).

As per claim 21 the means for deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word comprises a chip combiner 73 configured to derive a more accurate symbol estimate for a sliced chip, and wherein the chip combiner provides improved symbol estimates to the means for slicing chip.

As per claim 22, see claim 14.

As per claim 24, Webster teaches updating at least one previously determined chip slice identification based on the identification of the sliced chip and wherein the determining the noise component is based on the updated previously determined chip sliced identification and the identification of the chip slice see fig. 5.

As per claim 25, see claim 14.

As per claim 26, the feedback filter comprises a plurality of content registers and the chip slicer is configured to update at least one of the content registers based on the chip value see fig. 8.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webster.

As per claim 15, Webster et al teaches every feature of the claimed invention but does not explicitly teach the coefficients for the feed forward filter and the feedback filter are selected based on minimum mean square error (MMSE) criterion using either adaptive techniques or based on computations involving a channel estimate. However it is well known in the art for equalizer to generate coefficients for the feed forward filter and the feedback filter are selected based on minimum mean square error (MMSE)

criterion using either adaptive techniques or based on computations involving a channel estimate. Given that, it would have been obvious to one skilled in the art to calculate coefficients for the feed forward filter and the feedback filter are selected based on minimum mean square error (MMSE) criterion using either adaptive techniques or based on computations involving a channel estimate so as to take advantage of its enhanced technical feature such as reduced complex processing.

As per claim 23, it would have been obvious to one skill in the art to use the code words as CCK codewords in order to satisfy desired coding requirements.

RESPONSE TO ARGUMENTS

10. Applicant's arguments filed 9/1/06 have been fully considered but they are not persuasive. It is alleged that the office action contends that Webster describes the claimed feature "deriving a more accurate estimate for the sliced chip based on a correlation among the chips in the codeword" in the coherent matched filter 33. However, it is note that the office action clearly estates that the claim feature is met by the combiner 73 responsive to the output of the matched filter 33. It is further alleged that Webster does not teach any element that determined an estimate based on a correlation among the chips in a codeword. However, it is noted at page 3, line 2 of applicant's own disclosure, the chips are inherently correlated in a codewords" hence the estimate teaches by Webster is inherently based on correlation among the chips in a codeword since the chips are inherently correlated in a codeword.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Corrielus whose telephone number is 571-272-3020. The examiner can normally be reached on Maxi-Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean B Corrielus
Primary Examiner
Art Unit 2611 10.16.06